ABSTRACT OF THE DISCLOSURE

The present invention is generally directed to an improved automatic test pattern generator for generating test patterns that are used by an integrated circuit testing device. In accordance with one aspect of the invention, a method is provided for generating a set of test vectors for testing an integrated circuit, each test vector of the set of test vectors containing a plurality of bits defining test inputs for the integrated circuit. The method includes the steps of defining a list of faults for the integrated circuit, and generating at least one test vector that defines values for those inputs necessary to detect at least one target fault selected from the list of faults, the values comprising only a portion of the bits of the at least one test vector, wherein a remainder of the bits in the at least one test vector are unspecified bit positions. The method further includes the step of setting the values of a plurality of the unspecified bit positions using a non-random filling methodology.